ESD ASSOCIATION REGIONAL TUTORIALS

June 29-30, 2016

Plaza Suites Hotel, 3100 Lakeside Drive, Santa Clara, CA, USA

Lunch and refreshments provided

Register Online at www.esda.org/events/calendar/

Co-Sponsored by Sanwei ESD Solution USA

June 29-30, 2016

ESD DEVICE DESIGN ESSENTIALS

8:00 a.m. - 5:00 p.m.

Instructors: Gianluca Boselli, Texas Instruments;
Michael Khazhinsky, Silicon Laboratories

Gianluca Boselli

Michael Khazhinsky

This two-day seminar consists of concentrated versions of twelve ESDA tutorials which comprise the ESDA Device Design Certification Program.

- ESD On-Chip Protection in Advanced Technologies
- SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits
- EOS/ESD Failure Models and Mechanisms
- On-Chip ESD Protection in RF Technologies
- Charged Device Model Phenomena and Design
- Latch-up Physics and Design
- Circuit Modeling and Simulation for On-Chip Protection
- Troubleshooting On-Chip ESD Failures
- Device Testing--IC Component Level: HBM, CDM, MM, and TLP
- Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design
- Transmission Line Pulse Measurements: Parametric Analyzer for ESD On-Chip Protection
- System Level ESD/EMI: Testing to IEC and other Standards

DAY 1 June 29th

PART I (8:00 AM-Noon)

This part reviews the fundamentals of ESD testing, high-current physics, and ESD modeling. The focus is on device-level (HBM, CDM, MM, TLP) and system level testing, impact of technology scaling on ESD high current phenomena, as well as circuit modeling and simulation for on-chip protection.

PART II (1:00 PM-5:00)

The principles from part I are then applied to ESD Protection Design. This part describes ESD on-chip protection in advanced technologies, SPICE-based ESD protection design utilizing diodes, and active MOSFET rail clamp circuits.

DAY 2 June 30th

PART III (8:00 AM-Noon)

This part describes special ESD design cases, including Charged Device Model (CDM) phenomena and design, on-chip ESD protection in RF Technologies, and latch-up physics and design.

PART IV (1:00 PM-5:00)

The final section discusses EOS/ESD failure models and mechanisms. The seminar concludes with practical examples for troubleshooting of on-chip ESD failures.

Setting the Global Standards for Static Control!

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June 29-30, 2016
Essentials for ESD Programs
Factory: Technologies • Controls • Procedures
8:00 a.m. - 5:00 p.m.

Instructors: Ted Dangelmayer, Dangelmayer Associates LLC
Terry Welsher, Dangelmayer Associates LLC

Ted Dangelmayer

Terry Welsher

This two-day seminar consists of concentrated versions of the 10 ESDA tutorials which comprise the ESDA Program Manager (PrM) Certification Program:

- ESD Basics for the Program Manager
- Ionization and Answers for the Program Manager
- Packaging Principles for the Program Manager
- System Level ESD/EMI: Testing to IEC and other Standards
- Cleanroom Considerations for the Program Manager
- How To's of In-Plant ESD Survey and Evaluation Measurements
- Device Technology and Failure Analysis Overview
- Electrostatic Calculations for the Program Manager and the ESD Engineer
- ESD Standards Overview for the Program Manager
- ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)

Key concepts and information from the above courses have been selected for this two-day seminar. Many of the demonstrations and videos from ESD Basics Tutorial are included in this seminar. Examples of electrostatics and ESD calculations are included where appropriate throughout the seminar.

DAY 1 June 29th

PART I (8:00 AM-Noon)

This section reviews the fundamentals of electrostatics, charge flow, electric field and voltage. The concept of capacitance and the fundamental relationship, Q = CV, is introduced and explored with demonstrations and videos. The practical application of these concepts to the measurement of resistance, fields and voltages, and the relevant standards are reviewed and demonstrated.

PART II (1:00 PM-5:00)

The principles from Part I are then applied to grounding principles and standards, measurement of charge, standard models for ESD (i.e., human-body model and charged device model), and static induction with demonstrations and videos. Very simple and basic ESD protection circuit concepts and relevant failure analysis techniques are introduced and reviewed.

DAY 2 June 30th

PART III (8:00 AM-Noon)

Key ESD technical areas are reviewed such as air ionization, ESD-safe packaging, cleanroom principles and electrostatic attraction. Standards relevant to these areas are described.

PART IV (1:00 PM-5:00)

The final section includes charge generation test methods, additional ESDA standards, system-level ESD standards and testing, practical auditing techniques and strategies, and ESD event detection. The tutorial concludes with a review of ESD Protected-Areas (EPAs), ESD Program Management and the application of ANSI/ESD S20.20.

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About the Instructors:

Gianluca Boselli completed his Master in EE at the University of Parma, Italy, in 1996. In 2001 he completed his Ph.D. at the University of Twente, The Netherlands, where he worked on high current phenomena in CMOS technologies. In 2001 he joined Texas Instruments, Dallas, Texas, where he focused on ESD and Latch-up development for advanced CMOS technologies, with particular emphasis on process and modeling aspects. In 2007 his responsibilities extended into ESD development of Texas Instruments' Analog technologies portfolio, where he is now the manager of the Analog ESD Team. He authored several papers in the area of ESD and Latch-up. He presented his work at major conferences, including EOS/ESD Symposium, IEDM, and IRPS. He also presented many invited tutorials and papers at various conferences, including EOS/ESD Symposium, IRPS, IEDM, ESREF, IEW and RCJ. Dr. Boselli has been the recipient of the "Best Paper Award" on behalf of Microelectronics Reliability Journal in 2000. He received "The Best Paper Award" at the EOS/ ESD Symposium 2002. He also received the "Outstanding Symposium Award" at the EOS/ESD Symposium in 2002, 2006 and 2010. Dr. Boselli served multiple times as Sub-Committee Chair for Technical Program Committees (TPC) of EOS/ESD Symposium, IRPS, IEW and ESREF. He served as moderator and panelist in many workshops in ESD and Latch-up area. Dr. Boselli has served as TPC Chair at the EOS/ESD Symposium 2006, Vice-General Chair at the EOS/ESD Symposium 2007 and General Chair at the EOS/ESD Symposium 2008. He is currently President of the EOS/ESD Association. Dr. Boselli is an IEEE senior member and holds seventeen patents with several pending. Dr. Boselli serves in the Editorial Board of the IEEE Transactions on Device and Materials Reliability (T-DMR).

Ted Dangelmayer is the president of Dangelmayer Associates, LLC and has assembled an ESD consulting team consisting of the foremost authorities in virtually all ESD areas of both product design and manufacturing. He received the "Outstanding Contribution" award and the EOS/ESD Association "Founders" award. He was president of the EOS/ESD Association, chairman of the ESDA standards committee, and general chairman of the EOS/ESD Symposium. He has published two editions of his book, ESD Program Management, numerous magazine articles, and technical papers. Ted holds three patents and is iNARTE certified. He is currently president of the Northeast local chapter of the ESD Association and a member of the education committee.

Michael Khazhinsky is currently a Senior ESD staff engineer/designer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he worked at Motorola and Freescale Semiconductors where he was in charge of the TCAD development and ESD/latchup protection solutions for emerging process technologies, with a focus on ESD-EDA. Michael has M.S.E.E. and M.S. Physics from the Moscow State Institute of Electronic Engineering, and Ph.D. in Physics from Western Michigan University. Michael served as a member of the IRPS, IPFA and EOS/ESD Symposium Technical Program Committees, as well as a Workshop Chair, Technical Program Chair, Vice General Chair and General Chair of EOS/ESD Symposium. Michael co-authored over 30 external papers and gave a number of invited talks on ESD, EDA, process/device TCAD, and photonic crystals. He was a co-recipient of six EOS/ESD Symposium and SOI Symposium "Best Paper" and "Best Presentation" awards. Michael currently holds sixteen patents on ESD design, with additional patents pending. Michael is a Senior Member of IEEE and the elected Director of the EOS/ESD Association.

Terry Welsher is currently Senior Vice President of Dangelmayer Associates. He began his career in Bell Labs in 1978 where he worked on electrolytic corrosion failure mechanisms in electrical interconnection materials. In 1986 he began directing Bell Laboratories' core expertise in electrostatic discharge (ESD). The newly formed group proceeded to produce a string of ground-breaking contributions to the field and played a key role in advancing industry standards. At his retirement from Lucent Bell Labs in 2001, he was Director of the Quality, Reliability and Test Center of Excellence. Dr. Welsher has served as Chairman of the ESDA Standards Committee and Technical Program and General Chair of the EOS/ESD Symposium. He has also been active in the JEDEC Quality and Reliability Committee and Board of Directors and a member of the iNARTE Board of Directors. Most recently he has led the effort to harmonize and merge JEDEC and ESDA device testing standards. He holds a B.S. in Chemistry from Florida State University and Ph.D. in chemical physics from the University of Texas at Austin. Terry and his wife, Karyl, live in Suwanee, Georgia.

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First Name: _____ Last Name: _____

Company Name: _____

Street: _____ City: _____

State/Province: _____ Country _____ Zip/Postal Code: _____

Address is (please check the one that applies) ☐ Home or ☐ Company

Phone: _____ Fax: _____ E-mail: _____

Course Selection

☐ **ESD DEVICE DESIGN ESSENTIALS** (June 29-30)	**$1710**
☐ **Essentials for ESD Programs-Factory: Technologies • Controls • Procedures** (June 29-30)	**$1710**

Register online at www.esda.org

Discount before May 13th: per 2 day Seminar $ 1510 / non-Members $1610

Cancellation & refund requests will be honored only if received in writing no later than May 13, 2016, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Payment Information

Payment is required at time of registration. Only checks drawn in U.S. currency on a U.S. bank that is a member of the Federal Reserve will be accepted; make checks payable to ESD Association.

Amount enclosed $ _____ ☐ Check ☐ Credit Card

Credit card type: ☐ Visa® ☐ Mastercard® ☐ American Express® ☐ Discover®

Credit card number: _____ Expiration date: _____

Name on card: _____ Security code: _____

Cardholder's signature: _____

Billing Address: _____

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